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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/441,380	11/16/1999	JERRELL P. HEIN	75622.P0007	4250

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EXAMINER	
SINGH, RAMNANDAN P	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/441,380	HEIN, JERRELL P.	
	Examiner	Art Unit	
	Ramnandan Singh	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-16* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. In view of the finding of new art, Final rejection dated Aug. 11, 2004 is withdrawn, prosecution is reopened, as new grounds of rejections are made.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chea, Jr. et al [US 4,456,991] in view of Kaplan [US 4,355,341].

Regarding claim 1, Chea, Jr. et al teach a method shown in Figs. 1-2, comprising:

sampling (i.e. using an analog-to-digital converter) at least one of a tip and a ring signal [Fig. 1, element 22; col. 4, lines 29-43] using amplifier (38) to determine a line voltage and a line current of a linefeed component (resistor 34 or resistor 36) of a subscriber loop [col. 5, line 49 to col. 6, line 3].

Chea, Jr. et al do not teach expressly calculating the instantaneous power of

a linefeed component and thereafter, applying this instantaneous power to determine a semiconductor junction temperature. However, it may be noted that the method of determining the temperature of a power device using the instantaneous power dissipation is well-known in the art.

Kaplan teaches computing an instantaneous power dissipation ($I_C x V_{CE}$) of transistor Q_P, a linefeed component [Fig. 1; col. 2, lines 15-38; col. 1, lines 19-39], and that the voltage across the semiconductor is proportional to the logarithm of the current therethrough. Kaplan further discloses determining the junction temperature of the semiconductor using the voltage across the semiconductor wherein voltage is proportional to temperature [col. 4, lines 32-63; col. 6, lines 18-25]. It is nevertheless a teaching to one of ordinary skill in the art to apply the same to other applications.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the temperature determining technique of Kaplan with Chea, Jr. et al.

The suggestion/motivation for doing so would have been to limit the power dissipation in a transistor (i.e. a component of a subscriber loop shown in Fig. 2 of Chea, Jr. et al) in order to protect such transistor from damage [Kaplan; col. 1, lines 11-13].

Claim 5 is essentially similar to Claim 1 and is rejected for the reasons stated above.

Claim 7 is also essentially similar to Claim 1 except for an analog-to-digital converter (ADC) for sampling at least one of a Tip signal and a RING signal. Chea, Jr. et al teach an analog-to-digital converter using codec/filter (22), as shown in Fig. 1 [col. 4, lines 29-43].

Regarding claims 2, 6 and 8, Kaplan teaches a threshold comparator 16 to compare the voltage sum on conductor 30 to a reference potential V_{REF} supplied on conductor 28 for protecting transistor Q_P. This threshold voltage represents an alarm temperature the component [Figs. 1-3; col. 2, lines 4-14; col. 2, lines 32-42; col. 4, lines 44-49; col. 5, lines 3-9].

Regarding claim 3, Chea, Jr. et al teach timesharing a same monitor circuitry [Fig. 2; col. 7, line 26 to col. 8, line 2] to perform the steps as outlined in claim 1 above in combination with Kaplan. As a result, the combination of Chea, Jr. et al and Kaplan can monitor each linefeed component connected to the subscriber loop interface.

Regarding claim 4, the combination of Chea, Jr. et al and Kaplan teaches programming (i.e. logic control using software) a filter (i.e. a signal processor) [Chea, Jr. et al ; col. 10, lines 18-36] and a control and data interface (12) for combining filtering

parameters (22) [Chea, Jr. et al; col. 12, lines 43-54], corresponding to thermal characteristics of the linefeed component [Kaplan; Fig. 1; col. 2, lines 15-38; col. 1, lines 19-39].

Regarding claim 9, the combination of Chea, Jr. et al and Kaplan teaches the apparatus comprising;

a multiplexer/demultiplexer (12) coupling at least one tip and ring signals to the ADC (22) [Chea, Jr. et al; Fig. 1; col. 4, lines 53-65; col. 16, lines 3-8] to enable providing an estimated junction temperature of any of the linefeed components using the same ADC, power calculator, and filter [Kaplan; Fig. 1; col. 2, lines 15-38; col. 1, lines 19-39].

Regarding claims 10-11, the limitations are shown above.

Regarding claim 12, Chea, Jr. et al teach a non-volatile memory (NMRAM) wherein parameters and a program could be stored [Fig. 4; col. 12, lines 43-54].

Allowable Subject Matter

4. Claims 13-16 are allowable.

Examiner's Statement of Reasons for Allowance:

Claim 13 identifies the uniquely distinct feature of a subscriber loop interface circuit apparatus comprising: a signal processor having sense inputs for receiving a sensed tip signal and a sensed ring signal from a tip line and a ring line of a subscriber loop; and a linefeed driver for driving the subscriber loop in according with the subscriber loop control signals, the linefeed driver including a tip fuse series-coupled to the tip line and a ring fuse series-coupled to the ring line , wherein the sensed tip signal includes first and second sampled tip voltages sampled from opposing sides of the tip fuse, wherein the sensed ring signal includes first and second sampled ring voltages sampled from opposing ends of the ring fuse, as shown in Applicant's figures 3 and 5. As such, claim 13 requires a sensed tip signal including first and second sampled tip voltages sampled from opposing sides of the tip fuse and a sensed ring signal including first and second sampled ring voltages sampled from opposing ends of the ring fuse. While the closest prior art, Halbig [US 4,856,059], Chea, Jr. et al [US 4,456,991], Kaplan [US 4,355,341], and Patel [US 4,982,307] each teaching sensing signals for estimating power dissipation, Halbig sensing inputs for receiving a sensed tip signal and a sensed ring signal, Kaplan estimating an instantaneous power dissipation of a transistor, Chea, Jr. et al sampling a tip and a ring signal to determine a line voltage and a line current, and Patel sensing inputs from a tip and a ring; none of them suggest a sensed tip signal including first and second sampled tip voltages sampled from opposing sides of the tip fuse or a sensed ring signal including first and second sampled ring voltages sampled from opposing ends of the ring fuse. As such, the prior

art, either singularly or in combination, fail to anticipate or render the above underlined limitation obvious. Therefore, claim 13 is allowable.

Claims 15 and 16 are essentially similar to claim 13 and hence they are allowable.

Claim 14 is allowable due to dependence from claim 13.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(i) Chea, Jr. [US 4,317,963] teaches a subscriber line interface circuit (SLIC) for reducing power dissipation in the SLIC [Figs. 1-9; Abstract].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ramnandan Singh whose telephone number is (571) 272-7529. The examiner can normally be reached on M-TH (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ramnandan Singh
Examiner
Art Unit 2646

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SINH TRAN
SUPERVISORY PATENT EXAMINER